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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,571	09/25/2004	Jeng-Shu Liu	13566-US-PA	5570

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,571	LIU ET AL.	
	Examiner	Art Unit	
	Terrence R. Willoughby	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 and 9-12 is/are rejected.

7)☒ Claim(s) 7-8 and13-24 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 September 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures (1A, 1B, and 1C) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 1, paragraph 5 of the specification the phrase "level shifter **110**" should be rewritten as "level shifter 120" to be consistent with the drawing figures. Also, on page 8 paragraph 40 of the specification the phrase "the first ground **circuit** VSS1" should be change to "the first ground voltage VSS1" to be consistent with the drawing figures.

Appropriate correction is required.

Claim Objections

3. Claim 23 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

4. Claim 19 is objected to because of the following informalities: The phrase "ablelevel" needs a space between the two words.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0135206 A1) (hereinafter "Kato-206") in view of Kato (US 2003/0116806 A1) (hereinafter "Kato-806").

7. Regarding claim 1, Kato-206 in (Fig. 1) discloses a electrostatic discharge (ESD) preventing-able level shifter, for receiving a first signal and outputting a second signal with a level corresponding to a level of the first signal, the first signal being transmitted (para, [0017]) between a first system voltage (VDD-A) and a first ground voltage (GND-A), and the second signal being transmitted between a second system voltage (VDD-B) and a second ground voltage (GND-B), the level shifter comprising:

an inverter (Tr1, Tr2, Tr5, Tr6) for receiving the first signal and outputting a first reverse signal, wherein the first reverse signal is reverse with respect to the first signal and is transmitted between the first system voltage (VDD-A) and a first ground voltage (GND-A);

a voltage converter (Tr3, Tr4, Tr7, Tr8) wherein a first input terminal (Tr7) of the voltage converter is adapted for receiving the first reverse signal, a second input terminal (Tr8) of the voltage converter is adapted for receiving the first signal and an output terminal of the voltage converter is adapted for outputting the second signal;

a first ESD clamp transistor (Tr10) connected between the first system voltage (VDD-A) and first ground voltage (GND-A);

a second ESD clamp transistor (Tr11) connected between the second system voltage (VDD-B) and the second ground voltage (GND-B);

a third ESD clamp transistor (Tr9) connected between the first ground voltage (GND-A) and the second ground voltage (GND-B).

Kato-206 does not disclose a first ESD clamp circuit, wherein a first terminal of the first a first ESD clamp circuit, wherein a first terminal of the first ESD clamp circuit is coupled to the first input terminal of the voltage converter and a second terminal of the first ESD clamp circuit is coupled to the second ground voltage; and

a second ESD clamp circuit, wherein a first terminal of the second ESD clamp circuit is coupled to the second input terminal of the voltage converter and a second terminal of the second ESD clamp circuit is coupled to the second ground voltage.

Kato-806 discloses in (Figs. 4-9) an input protection circuit of a semiconductor apparatus, and more particularly to an electrostatic destruction prevention protection circuit (abstract) formed between a input terminal/signal line (1,13) and power source potential line (2) or ground potential line (3) and a internal inverter circuit (50) wherein

the electrostatic destruction prevention protection circuit comprises ESD clamping circuits (10,14,16,17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD preventing-able level shifter device of Kato-206 with the ESD clamping teachings of Kato-860 which is coupled to the first and second input terminal of the voltage converter and to the second ground voltage to effectively protect the input and output terminals of the semiconductor apparatus, particularly the gate oxide film of the inverter which is most vulnerable to surge currents.

8. Regarding claim 2, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 1, wherein the first ESD clamp circuit (Kato-806, Fig. 4, 10) comprises an N-type transistor (Kato-806, para. [0039]), wherein a drain of the N-type transistor is coupled to the first input terminal of the voltage converter (Kato-206, Fig. 1, Tr3, Tr4, Tr7, Tr8), and wherein a gate, source and a bulk of the N-type transistor (Kato-806, 10) are coupled to the second ground voltage (Kato-206, Fig. 1, GND-B).

9. Regarding claim 3, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 1, wherein the first ESD clamp circuit comprises a transistor configured as a diode (Kato-806, Fig.4, 5,10). It is well known in the art that the transistor connected as disclosed in (Kato-806, Fig. 4, 5,10) is functional equivalent to a diode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the first clamping circuit comprising the diode/FET clamping teachings of Kato-206 to the ESD preventing-able level shifter of Kato-806

where a cathode of the diode is coupled to the first input terminal of the voltage converter and an anode of the diode is coupled to the second ground voltage to effectively protect the input and output terminals of the semiconductor apparatus, particularly the gate oxide film of the inverter which is most vulnerable to surge currents.

10. Regarding claim 4, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 1, wherein the inverter comprises:

a P-type transistor (Kato-206, Fig. 1, Tr1), wherein a source of the P-type is coupled to the first system voltage (Kato-206, Fig. 1, VDD-A), a gate of the P-type transistor is adapted for receiving the first signal, a drain of the P-type transistor is adapted for outputting the first reverse signal (Kato-206, para. [0017]); and

an N-type transistor, (Kato-206, Fig. 1, Tr5), wherein a gate of the N-type transistor is adapted for receiving the first signal, a drain of the N-type transistor is coupled to the drain of the P-type transistor, a source of the N-type transistor is coupled to the first ground voltage (Kato-206, Fig. 1, GND-A).

11. Regarding claim 5, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 1, wherein the voltage converter comprises:

a first transistor (Kato-206, Fig. 1, Tr3), wherein a first drain/source of the first transistor is coupled to the second system voltage (Kato-206, Fig. 1, VDD-B);

a second transistor (Kato-206, Fig. 1, Tr7), wherein a gate of the second transistor is adapted for receiving the first reverse signal, a first source/drain of the second transistor is coupled to a second source/drain of the first transistor (Kato-206,

Fig. 1, Tr3) and a second source/drain terminal of the second transistor is coupled to the second ground voltage (Kato, 206, Fig. 1, GND-B);

a third transistor (Kato-206, Fig. 1, Tr4), wherein a first source/drain of the third transistor is coupled to the second system voltage (Kato-206, Fig. 1, VDD-B), a second source/drain of the third transistor is coupled to the gate of the first transistor (Kato-206, Fig. 1, Tr3) and a gate of the third transistor is coupled to the second source/drain of the first transistor; and

a fourth transistor (Kato-206, Fig. 1, Tr8), wherein a gate of the fourth transistor is adapted for receiving a first signal, a first source/drain of the fourth transistor is coupled to the second source/drain of the third transistor (Kato-206, Fig. 1, Tr4) and a second source/drain of the fourth transistor is coupled to the second ground voltage (Kato-206, Fig. 1, GND-B), and wherein a signal of the first source/drain of the fourth transistor is the second signal.

12. Regarding claim 6, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 5, wherein the first and third transistors are P-type transistors (Kato-206, Fig. 1, Tr3, Tr4) and the second and fourth transistors are N-type transistors (Kato-206, Fig. 1, Tr7, Tr8).

13. Regarding claim 9, Kato-206 in view of Kato-806 discloses a electrostatic discharge (ESD) preventing-able level shifter, for receiving a first signal and outputting a second signal with a level corresponding t Kato-206, Fig. 1,o a level of the first signal, the first signal being transmitted (Kato-206 and para, [0017]) between a first system voltage (Kato-206, Fig. 1, VDD-A) and a first ground voltage (Kato-206, Fig. 1,GND-A),

and the second signal being transmitted between a second system voltage (Kato-206, Fig. 1,VDD-B) and a second ground voltage (Kato-206, Fig. 1,GND-B), the level shifter comprising:

an inverter (Kato-206, Fig. 1,Tr1, Tr2, Tr5, Tr6) for receiving the first signal and outputting a first reverse signal, wherein the first reverse signal is reverse with respect to the first signal and is transmitted between the first system voltage (Kato-206, Fig. 1,VDD-A) and a first ground voltage (Kato-206, Fig. 1,GND-A);

a voltage converter (K Kato-206, Fig. 1,ato-206, Fig. 1, Tr3, Tr4, Tr7, Tr8) wherein a first input terminal (Kato-206, Fig. 1,Tr7) of the voltage converter is adapted for receiving the first reverse signal, a second input terminal (Kato-206, Fig. 1,Tr8) of the voltage converter is adapted for receiving the first signal and an output terminal of the voltage converter is adapted for outputting the second signal;

a first ESD clamp transistor (Kato-206, Fig. 1,Tr10) connected between the first system voltage (Kato-206, Fig. 1,VDD-A) and first ground voltage (Kato-206, Fig. 1,GND-A);

a second ESD clamp transistor (Kato-206, Fig. 1,Tr11) connected between the second system voltage (Kato-206, Fig. 1,VDD-B) and the second ground voltage (Kato-206, Fig. 1,GND-B);

a third ESD clamp transistor (Kato-206, Fig. 1,Tr9) connected between the first ground voltage (Kato-206, Fig. 1,GND-A) and the second ground voltage (Kato-206, Fig. 1,GND-B).

Kato-206 does not disclose a first ESD clamp circuit, wherein a first terminal of the first a first ESD clamp circuit, wherein a first terminal of the first ESD clamp circuit is coupled to the second system voltage and a second terminal of the first ESD clamp circuit is coupled to the first input terminal of the voltage converter; and

a second ESD clamp circuit, wherein a first terminal of the second ESD clamp circuit is coupled to the second system voltage and a second terminal of the second ESD clamp circuit is coupled to the second input terminal of the voltage converter.

Kato-806 discloses in (Figs. 4-9) an input protection circuit of a semiconductor apparatus, and more particularly to an electrostatic destruction prevention protection circuit (abstract) formed between a input terminal/signal line (1,13) and power source potential line (2) or ground potential line (3) and a internal inverter circuit (50) wherein the electrostatic destruction prevention protection circuit comprises ESD clamping circuits (10,14,16,17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ESD preventing-able level shifter device of Kato-206 with the ESD clamping teachings of Kato-860 which would be coupled to the first and second input terminal of the voltage converter and to the second ground voltage to effectively protect the input and output terminals of the semiconductor apparatus, particularly the gate oxide film of the inverter which is most vulnerable to surge currents.

14. Regarding claim 10, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 9, wherein the first ESD clamp circuit (Kato-806, Fig. 9, 17)

comprises an P-type transistor (Kato-806, para. [0039]), wherein a drain of the P-type transistor is coupled to the first input terminal of the voltage converter (Kato-206, Fig. 1, Tr3, Tr4, Tr7, Tr8), and wherein a gate, source and a bulk of the P-type transistor (Kato-806, Fig. 9, 17) are coupled to the second system voltage (Kato-206, Fig. 1, VDD-B).

15. Regarding claim 12, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 9, wherein the inverter comprises:

a P-type transistor (Kato-206, Fig. 1, Tr1), wherein a source of the P-type is coupled to the first system voltage (Kato-206, Fig. 1, VDD-A), a gate of the P-type transistor is adapted for receiving the first signal, a drain of the P-type transistor is adapted for outputting the first reverse signal (Kato-206, para. [0017]); and

an N-type transistor, (Kato-206, Fig. 1, Tr5), wherein a gate of the N-type transistor is adapted for receiving the first signal, a drain of the N-type transistor is coupled to the drain of the P-type transistor, a source of the N-type transistor is coupled to the first ground voltage (Kato-206, Fig. 1, GND-A).

16. Claim 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0135206 A1) (hereinafter "Kato-206") in view of Kato (US 2003/0116806 A1) (hereinafter "Kato-806") as applied to claims 1 and 9 above, and further in view of Takeda et al. (US 6,385,021).

17. Regarding claim 11, Kato-206 in view of Kato-806 discloses the ESD preventing-able level shifter of claim 9, wherein the first ESD clamping circuit comprises a diode/FET transistor (Kato-206, Fig. 4, 5,10).

Kato-206 in view of Kato-806 does not disclose an anode of the diode is coupled to the first input terminal of the voltage converter and a cathode of the diode is coupled to the second system voltage.

Takeda et al. in (Fig. 2) disclose an electrostatic discharge protection circuit wherein the diodes (26,27) are connected between the input/output (23) terminals and the positive power supply rail (21) or the negative power supply rail (22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the diode clamping teachings of Takeda et al. to the ESD preventing-able level shifter of Kato-206 and Kato-806 where the anode of the diode is coupled to the first input terminal of the voltage converter and a cathode of the diode is coupled to the second system voltage to protect the input and output terminals of the semiconductor apparatus (i.e. integrated circuits) that is most susceptible to damages during positive and negative ESD events.

Allowable Subject Matter

18. Claims 7-8 are objected to as being dependent upon a rejected base claim 1, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 7 would be allowable over the prior art of record because the prior art does not teach or suggest a fifth transistor, wherein a gate of the fifth transistor is coupled to the gate of the fourth transistor and a first source/drain of the fifth

transistor is coupled to the second source/drain of the fourth transistor; and a sixth transistor, wherein a gate of the sixth transistor is coupled to the second source/drain of the first transistor, a first source/drain of the sixth transistor is coupled to a second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fifth transistor is the second signal as set forth in the claimed invention.

19. Claims 13-14 are objected to as being dependent upon a rejected base claim 9, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 13 would be allowable over the prior art of record because the prior art does not teach or suggest wherein a gate of the fifth transistor is adapted for receiving the first signal, a first source/drain of the fifth transistor is coupled to the second source/drain of the fourth transistor and a second source/drain of the fifth transistor is coupled to a gate of the first transistor; and a sixth transistor, wherein a gate of the sixth transistor is adapted for receiving the first signal, a first source/drain of the sixth transistor is coupled to a second source/drain of the fifth transistor and a second source/drain of the sixth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the sixth transistor is the second signal as set forth in the claimed invention.

20. Claims 15-16 are objected to as being dependent upon a rejected base claim 9, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 15 would be allowable over the prior art of record because the prior art does not teach or suggest a third transistor, wherein a first source/drain of the third transistor is coupled to the second system voltage, a second source/drain voltage is coupled to the gate of the second transistor and a gate of the third transistor is adapted for receiving the first signal; and a fourth transistor, wherein a gate of the fourth transistor is coupled to the second source/drain of the first transistor, a first source/drain of the fourth transistor is coupled to the second source/drain of the third transistor and a second source/drain of the fourth transistor is coupled to the second ground voltage, and wherein a signal of the first source/drain of the fourth transistor is the second signal.

21. Claims 17-18 are objected to as being dependent upon a rejected base claim 9, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claim 17 would be allowable over the prior art of record because the prior art does not teach or suggest the fifth and sixth transistor structural configuration as set forth in the claimed invention.

22. Claims 19-24, the following is a statement of reasons for the indication of allowable subject matter: The prior art record failed to teach or suggest an ESD clamp circuit, wherein a first terminal of the ESD clamp circuit is coupled to the second system voltage and a second terminal of the ESD clamp circuit is coupled to the first ground voltage as set forth in the claimed invention.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kato (US 6,608,744) in (Fig. 1 and 2) discloses an SOI CMOS input protection circuit with open-drain configuration (abstract) comprising a transistor (26) configured as a diode (28). Rizzi et al. (US 3,848,238) discloses a conversion of a bipolar transistor into a diode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TRW
1/31/07

Stephen W Jackson
2-1-07

STEPHEN W. JACKSON
PRIMARY EXAMINER